Design and Process Sensitivity of a Two-Stage 6–18-GHz Monolithic Feedback Amplifier

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Abstract—**The design of a 6–18-GHz two-stage monolithic feedback amplifier is discussed, and the critical process and FET parameters are identified. Variations in circuit performance experienced during a pilot production run are correlated with the predictions of a sensitivity analysis. Five circuit model parameters were selected for study: substrate height, GaAs sheet resistance, gate-source capacitance, transconductance, and drain-source resistance. Measured results show the importance of substrate height and sheet resistance in the control of gain flatness. An example on-slice RF performance distribution is presented, showing the suitability of the circuit and fabrication process for high-volume production.**

I. Introduction

UNDERSTANDING THE effects of material and process parameter variations on circuit performance is crucial to the development of high-volume MMIC manufacturing capability. The circuit design and fabrication process must work together to produce large quantities of MMIC chips with acceptable RF performance. At Texas Instruments, we have evaluated the RF performance of two-stage monolithic feedback amplifier chips from over 60 slices. In this paper, we discuss efforts to control the gain ripple of pilot production chips made using our most recent design, and present an example distribution of on-slice RF performance.

Two sets of variables emerge in the study of MMIC producibility: the equivalent circuit model parameters used by the design engineer, and raw physical characteristics such as the velocity-field relationships, doping concentrations, etch rates, and contact resistances familiar to the device physicist and process engineer. Ultimately, analysis of yield and producibility must trace RF performance directly to the material and process parameters, but such an analysis is beyond the scope of this paper. We focus instead on the circuit engineer's point of view, in particular on the effort required to identify and correct problem areas in a new MMIC design.

II. Design Description

The monolithic feedback amplifier shown in Fig. 1 is designed for use as a broad-band, low to medium power gain stage. Henceforth, we refer to the device by its Texas Instruments Equipment Group part number, EG8005. Feedback is used as a mechanism for gain flattening and VSWR reduction, and the cascaded common-source configuration enables the device to attain more than 10-dB gain across the 6–18-GHz band with medium power-added efficiency. Some EG8005 devices have achieved 17-percent p.a.e. at 18 GHz, when operated with 21-dBm output power at 1-dB gain compression. All blocking and bypass capacitors are provided on-chip. This design is a second iteration of the design presented in [1]; the performance deficiencies of the original design have been corrected along with a substantial reduction in chip area. Basic design data are shown in Table I.

The signal path in Fig. 1(b) is from left to right. The FET gatewidths are 300 μm. The two GaAs mesa feedback resistors can be seen near the gate pads. Only microstrip structures are used as tuning elements; there are no MIM or interdigitated tuning capacitors in the circuit. Gate and drain bias is applied through the four bond pads along the bottom of the chip. The square structures above the bond pads are 15-pF MIM bypass capacitors. The chip contains 85 pF of on-chip blocking and bypass capacitance.

The active layer is formed by ion implantation directly into semi-insulating substrates. The remainder of the fabrication process follows the approach described in [2]. The process employs mesa isolation, alloyed AuGeNiAu ohmic contacts, E-beam defined gates, Si_3N_4 MIM capacitors, Au plating with airbridges, and reactive ion etching for via hole fabrication.

III. Performance-Process Interactions

Gain responses of sample chips from an early slice, designated as slice A, are shown in Fig. 2. All samples were measured at a standard bias condition: −1.0-V gate to source and +6.0-V drain to source. The chips were selected on the basis of similar dc FET characteristics; the I_{dss} values for all the 300-μm FET's in each sample fell between 75 mA and 95 mA. The worst-case gain ripple for the sample is 5.08 dB and the average is 4.25 dB, over 6–19 GHz. A severe dip in the gain is apparent at 9.5 GHz.

Computer modeling of the circuit design resulted in the identification of five parameters that need to be well controlled in order to maintain consistent circuit perfor-

Manuscript received May 1, 1985; revised August 2, 1985.

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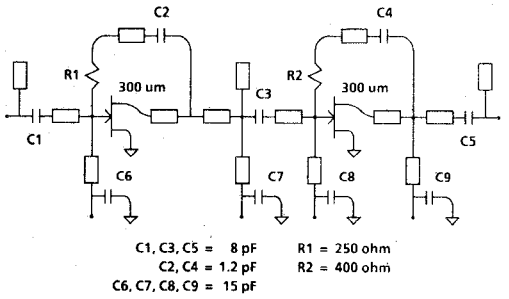
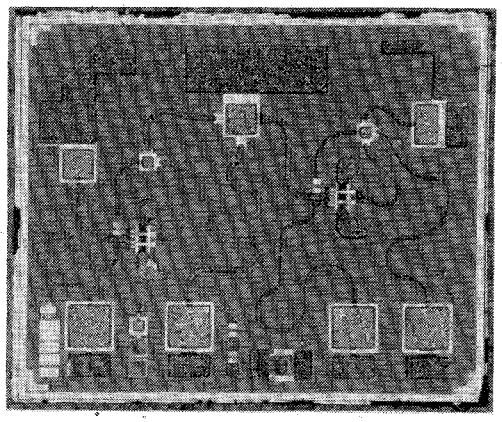


(a)



(b)

Fig. 1. The EG8005 two-stage feedback amplifier: (a) schematic, (b) photograph.

TABLE I
EG8005 DESIGN DATA

Chip Size: 92 × 75 mil

# of chips / slice	slice diameter	effective diameter
271	2 inch	1.8 inch
701	3 inch	2.8 inch

(allows for 6 mil saw streets and 10 test bars per slice)

Substrate thickness:	4.0 mil
Passivation/ Capacitor Dielectric:	2000 Å Silicon Nitride
Via Hole Diameter:	2.0 mil

Nominal Bias Conditions:

V_{DS}	6.0 V
V_{GS}	-1.0 V
I_{DS} (Total)	50-100mA

mance: FET intrinsic transconductance g_{mi}, gate-source capacitance C_{gs}, drain-source resistance R_{ds}, GaAs sheet resistance r_s, and substrate height h_s. A sensitivity matrix for the gain response at various frequencies is listed in Table II. The values in the table are estimates of the sensitivity factor S_G^α given by

$$S_G^\alpha = \frac{\alpha}{|S_{21}|}\frac{\partial |S_{21}|}{\partial \alpha}$$

where α is the parameter of interest and $|S_{21}|$ is the voltage gain of the amplifier. The sensitivity factors were obtained by perturbing the parameters in the computer model ± 10 percent and using a discrete approximation for the partial derivative. The factors can be thought of in this way: a 10-percent change in the parameter α causes a $10 \times S_G^\alpha$-percent change in voltage gain. Another example of sensitivity analysis is given in [3]. The normalized sensitivity factors provide a basis for the comparison of the sensitivities of different designs.

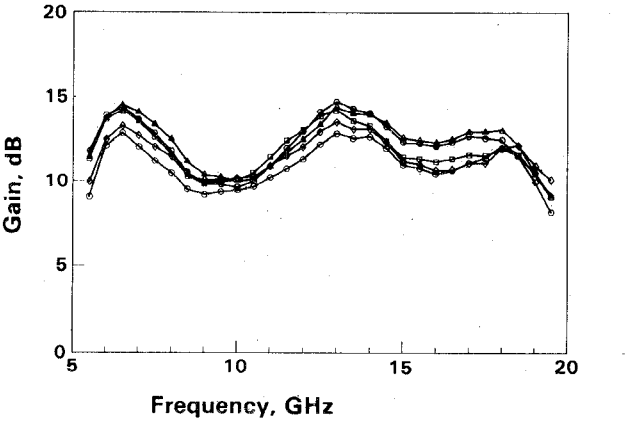


Fig. 2. Measured gain responses of selected amplifiers from slice A. All devices were measured at the standard bias condition $V_g = -1.0$ V, $V_d = +6.0$ V.

TABLE II
VOLTAGE GAIN SENSITIVITY FACTORS

$$S_G^\alpha = \frac{\alpha}{|S_{21}|}\frac{\partial |S_{21}|}{\partial \alpha}$$

parameter (α)	6.0 GHz	9.5 GHz	13.5 GHz	16.5 GHz	18.0 GHz
g_{mi}	1.52	1.72	1.67	1.79	1.82
C_{gs}	0.02	-0.30	-0.77	-1.06	-1.05
R_{ds}	0.38	0.26	0.48	0.41	0.43
r_s	0.99	0.48	0.39	0.05	0.00
h_s	0.01	0.58	0.34	0.12	-0.06

The effects of each type of parameter variation can be seen clearly in the matrix. Increases in transconductance simply translate the gain upward, although the effect is not completely uniform. Increases in gate-source capacitance reduce the high-end gain, but affect the low-end very little. Increases in drain-source resistance tend to accentuate the gain peak at 13.5 GHz and the dip at 9.5 GHz. Changes in the sheet resistance of the active GaAs layer affect the values of the feedback resistors (such changes affect the FET characteristics as well, but here the FET parameters are treated separately). Feedback is significant only in the lower half of the 6–18-GHz band; the effect of feedback resistor changes on the high-end gain is negligible. Increases in sheet resistance reduce the feedback effect, accentuating both the low-end peak and the dip at 9.5 GHz. Another prime suspect for the cause of the dip in gain at 9.5 GHz is the substrate height, which affects the dip region strongly.

Table III lists the values of the critical parameters assumed in the design, the values obtained from measure-

TABLE III
CRITICAL PARAMETER VALUES

symbol	units	design assumption	Slice A	Slice B
g_{mi}	mS	50	55	64
C_{gs}	pF	0 33	0 39	0 47
R_{ds}	Ω	250	292	285
r_s	Ω/□	400	552	336
h_s	mils	4 0	3 5	4 0

FET parameters at $V_{GS} = -1.0$ V, $V_{DS} = 6.0$ V.

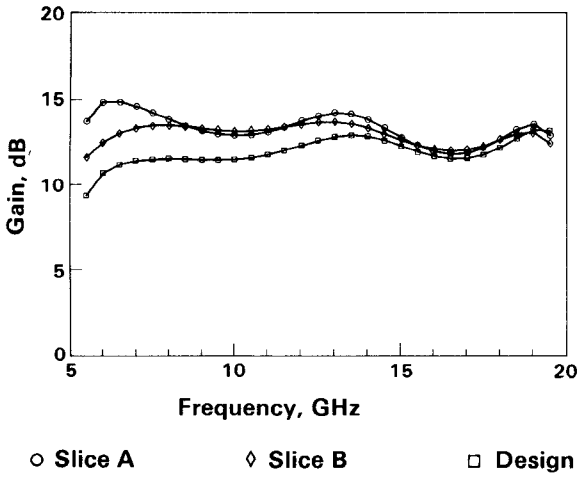


Fig. 3. Computer model responses for the original design, slice A, and slice B.

ments of slice A, and values obtained from a subsequent slice, designated as slice B. The computer model responses for these three cases are shown in Fig. 3, and the measured responses of the slice B amplifier samples are shown in Fig. 4. Intrinsic transconductance g_{mi} and the drain source resistance R_{ds} were calculated from low-frequency (100–400 MHz) scalar scattering parameter measurements of two sample FET's from each slice, neglecting the capacitive reactances and using dc values for the source and drain parasitic resistances R_s and R_d. The sample FET's were selected to have dc characteristics similar to those in the amplifier sample. The value of gate source capacitance for the two slices was simply adjusted to reflect the measured gain-slope characteristics of the amplifier samples. The sheet resistance variations were determined from measurements of the GaAs feedback resistors. A sample of five nonfunctional chips from the two slices was selected at random and cleaved in half for optical substrate height measurements. All the samples fell within ± 0.2 mils of the average value.

As can be seen in Fig. 3, despite careful attention to detail in the computer model of the circuit layout, we have been unable to predict all of the measured gain ripple. However, the trends predicted by the sensitivity analysis can be seen in the responses from slice B. The reduction in the feedback resistor values and the correction of the substrate height brought the worst-case gain ripple down

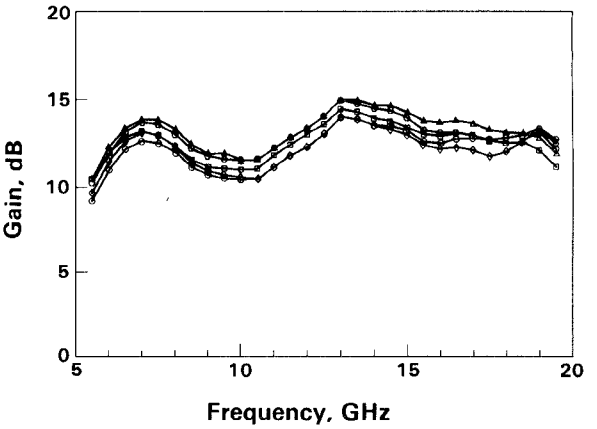


Fig. 4. Measured gain responses of selected amplifiers from slice B. All devices were measured at the standard bias condition $V_g = -1.0$ V, $V_d = +6.0$ V.

from 5.08 dB to 3.55 dB; the average gain ripple for the slice B sample is 3.47 dB.

The changes in g_{mi}, C_{gs}, and r_s suggest a higher implant activation for slice B, and indeed the process monitor C–V measurements did indicate a roughly 20-percent increase in the doping density under the gates of the slice B FET's. It is interesting to note that the overall level and slope of the gain responses are similar for the two slices, despite the changes in FET characteristics. Referring to the sensitivity matrix, note that at the high end of the band, the effect of the increase in g_{mi} is partially offset by the increase in C_{gs}; similarly, at the low end of the band, the increase in transconductance tends to be cancelled out by the downward change in r_s. Although we have considered adding a trim etch step to adjust the GaAs resistor values, it appears that allowing the resistors to vary helps reduce the sensitivity of the gain slope to variations in activation.

The sensitivity matrix suggests that a further adjustment to h_s might improve the response. A more recent sample with a 4.5-mil substrate height exhibited 3.27-dB average gain ripple. Further adjustments to h_s would probably increase gain ripple, however, due to a degradation of the input VSWR at the high end of the 6–18-GHz band.

IV. On-Slice RF Performance Distribution

Steady improvements in processing technique, inspired in part by experiences such as those discussed in the previous section, have resulted in higher yields and more uniform RF performance. The success of MMIC technology depends ultimately on the ability to achieve consistent microwave frequency performance. In this section, we discuss the process of "RF characterizing" a slice of MMIC's to determine the spread of RF performance parameters.

After completion of the fabrication process, a GaAs wafer is subjected to a visual inspection. The chips that pass visual inspection are given a final dc probe test; capacitors are checked for shorts, feedback resistances are measured, and the first- and second-stage FET saturation currents, breakdown voltages, and transconductances are measured. The engineer who selects chips for delivery is then faced with the task of deciding which chips are

TABLE IV
DC AND RF PARAMETERS OF MMIC SAMPLE AT 25° C

#	DC g_m, mS		$\|S_{21}\|$, dB		$\|S_{11}\|$, dB	$\|S_{22}\|$, dB	P_{out}, dBm*	NF, dB
	1st stage	2nd stage	MIN	MAX	MAX	MAX	MIN	MAX
1	50.0	52.0	11.67	14.48	-4.99	-6.02	13.60	6.38
2	50.0	50.0	11.86	14.63	-5.81	-6.20	12.66	7.03
3	49.0	50.0	11.46	14.70	-5.23	-5.32	13.93	6.56
4	46.2	47.5	10.80	13.71	-5.53	-5.26	13.38	6.69
5	44.0	42.5	9.10	12.74	-4.73	-4.65	10.47	6.75
6	40.0	39.0	6.79	10.46	-4.43	-5.37	8.10	9.88

* Output power at 1 dB gain compression

DC bias: $V_{GS} = -1.0$ V, $V_{DS} = 6.0$ V; Frequency Range: 6–18 GHz.

suitable for a given application. In the absence of a nondestructive means of RF testing each individual MMIC, the decision must be made based on dc probe data.

When the critical variables are well controlled, the most salient RF performance variation is the up-and-down translation in gain due to the strong transconductance sensitivity of the amplifier. At present, the best predictor of minimum small-signal gain appears to be simply the product of first- and second-stage dc transconductance $g_{m1}g_{m2}$. The dc transconductance is determined by observing the change in drain to source current I_{DS} as the gate to source voltage V_{GS} is varied from -0.8 V to -1.2 V, with the drain to source voltage, V_{DS} held at 2.0 V. The chips with higher transconductance tend to have lower noise figures and higher output power capabilities, as well as higher gain.

Below, we discuss specific results from a recent slice of EG8005's. A total of 102 chips from this slice passed visual inspection and dc probe. The substrate height had been adjusted as discussed in Section III; the average value from a sample of 10 measurements was 4.4 mil, with a standard deviation of 0.14 mil. The sheet resistance (estimated from measurements of the second-stage feedback resistances) averaged 450 Ω/□, with a standard deviation of 21 Ω/□. Six chips were selected from different parts of the $g_{m1}g_{m2}$ distribution, from best to worst. Table IV summarizes the results of the RF measurements, which were conducted at room temperature. Fig. 5 shows the frequency dependence of the RF performance parameters of a "typical" chip, #4. (It should be pointed out that the standard bias, $V_{GS} = -1.0$ V, $V_{DS} = 6.0$ V, is not necessarily the optimum one for a given application. For example, noise figure and gain ripple can be reduced by changing V_{DS} to 4.0 V, although this change reduces linear dynamic range as well.)

Fig. 6 illustrates the use of the sample chips to predict the distribution of minimum gain for the entire slice. The lower right-hand plot is a histogram of the $g_{m1}g_{m2}$ values for the 102 chips. The upper right-hand plot shows the correlation between the minimum value of $|S_{21}|$ in the 6–18-GHz band and $g_{m1}g_{m2}$. A least-squares fit of the data has been drawn on the graph; the correlation coefficient is 0.82. This fit has in turn been used to predict the minimum gain for the entire population of 102 chips. The distribution of predicted minimum gain is shown in the upper left-hand plot in Fig. 6. According to the prediction, 75 percent of the chips would meet a 10-dB minimum gain specification, and 90 percent would meet a 9.5-dB minimum gain specification.

Although a significant amount of on-slice performance variation is evident in the results, the variations tend to fall along predictable lines; chips can be sorted and selected based on dc probe data. A large majority of the chips in

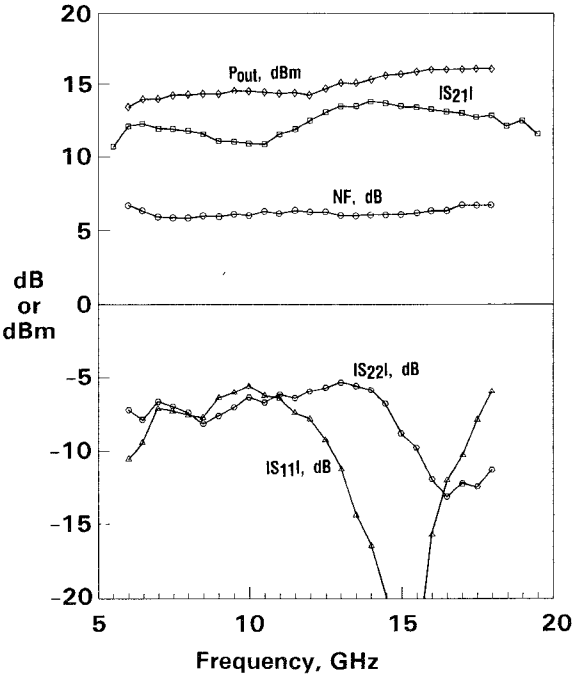


Fig. 5. RF performance of a "typical" chip, #4.

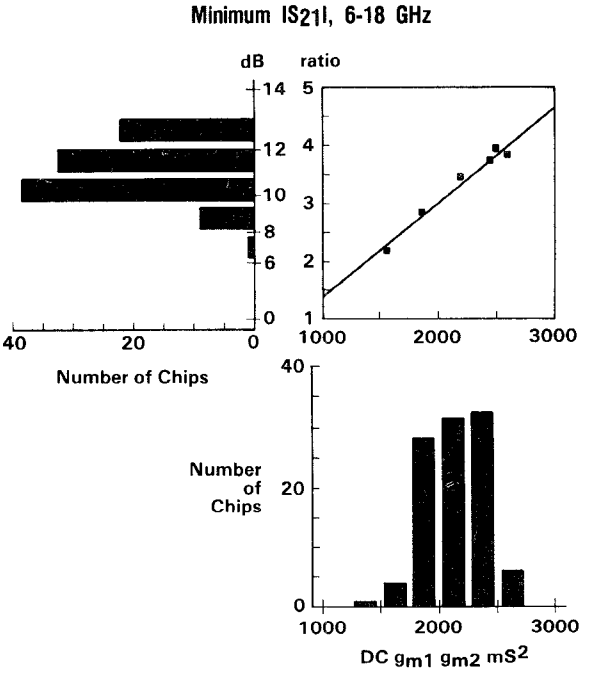


Fig. 6. Prediction of minimum small-signal gain from dc probe data.

this example can and will be used in experimental solid-state receiver modules.

V. Conclusions

Our present CAD software does not predict the EG8005 amplifier responses with extreme precision. When combined with the sensitivity analysis approach, however, it is very useful in tracking down problems and identifying ways to refine the small-signal response. This approach has resulted in substantial progress towards the goal of a mass-produced, standard, 6–18-GHz gain block.

Acknowledgment

The authors would like to acknowledge some of the many engineers who made important contributions to this work: D. Rhine, G. Boggan, G. Lerude, S. McCarter, and B. Mitchell.

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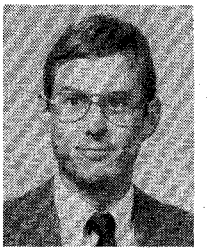

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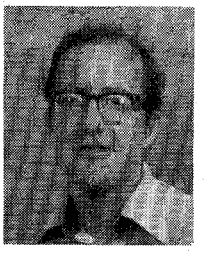

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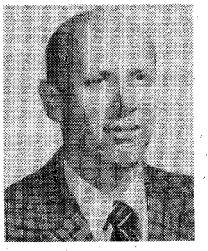

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